

# **JEDEC STANDARD**

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## **Definition of the SSTVN16857 2.5-2.6 V 14-Bit SSTL\_2 Registered Buffer for PC1600, PC2100, PC2700, and PC3200 DDR DIMM Applications**

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### **JESD82-3B.01**

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**JANUARY 2023**

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**STANDARD FOR DEFINITION OF THE SSTVN16857 2.5–2.6-V 14-BIT SSTL\_2  
REGISTERED BUFFER FOR DDR DIMM APPLICATIONS**

**(From JEDEC Board Ballot JCB-04-73, formulated under the cognizance of the JC-40 Committee on Digital Logic.)**

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## **1 Scope**

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This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTVN16857 14-bit SSTL\_2 registered buffer for PC1600, PC2100, PC2700, and PC3200 DDR DIMM applications.

The purpose is to provide a standard for the SSTVN16857 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

**NOTE** The designation SSTVN16857 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

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## **2 Device Standard**

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### **2.1 Description**

This 14-bit registered buffer is designed for 2.3-V to 2.7-V VDD (PC1600, PC2100, PC2700), and 2.6-V to 2.7-V VDD (PC3200) operation.

All inputs are compatible with the JEDEC standard for SSTL\_2, except the LVCMOS reset ( $\overline{\text{RESET}}$ ) input. All outputs are SSTL\_2, Class II compatible.

The SSTVN16857 operates from a differential clock (CK and  $\overline{\text{CK}}$ ). Data are registered at the crossing of CK going high, and  $\overline{\text{CK}}$  going low.

The device supports low-power standby operation. When  $\overline{\text{RESET}}$  is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage ( $V_{\text{REF}}$ ) inputs are allowed. In addition, when  $\overline{\text{RESET}}$  is low all registers are reset, and all outputs are forced low. The LVCMOS  $\overline{\text{RESET}}$  input must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied,  $\overline{\text{RESET}}$  must be held in the low state during power up.

In the DDR DIMM application,  $\overline{\text{RESET}}$  is specified to be completely asynchronous with respect to CK and  $\overline{\text{CK}}$ . Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers, thus ensuring no glitches on the output. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of  $\overline{\text{RESET}}$  until the input receivers are fully enabled, the design must ensure that the outputs will remain low.

Package options include plastic thin shrink small-outline, and plastic thin very small-outline (MO-153).

## 2 Device Standard (cont'd)

### 2.2 Pinout Figure

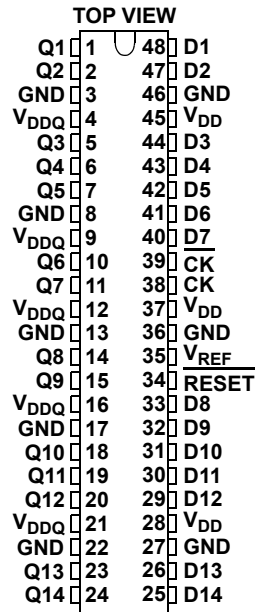


Figure 1 — 48-pin TSSOP Package and Pinout

### 2.3 Terminal functions

Table 1 — Terminal Functions

Terminal Name	Description		Electrical Characteristics
Q1–Q14	Data output		SSTL_2, Class II output
GND	Ground		Ground input
V <sub>DDQ</sub>	Output-stage drain power voltage	PC1600, PC2100, PC2700	2.5-V nominal
		PC3200	2.6-V nominal
V <sub>DD</sub>	Logic power voltage	PC1600, PC2100, PC2700	2.5-V nominal
		PC3200	2.6-V nominal
$\overline{\text{RESET}}$	Asynchronous reset input – resets registers and disables data and clock differential-input receivers		LVC MOS input
V <sub>REF</sub>	Input reference voltage	PC1600, PC2100, PC2700	1.25-V nominal
		PC3200	1.30-V nominal
CK	Positive main clock input		Differential input
$\overline{\text{CK}}$	Negative main clock input		Differential input
D1–D14	Data input – clocked in on the crossing of the rising edge of CK and the falling edge of $\overline{\text{CK}}$		SSTL_2 input

2 Device Standard (cont'd)

2.4 Function Table

Table 2 — Function Table (each Flip Flop)

Inputs				Q Outputs
$\overline{\text{RESET}}$	CK	$\overline{\text{CK}}$	D	
H	↑	↓	L	L
H	↑	↓	H	H
H	L or H	L or H	X	$Q_0$
L	X or Floating	X or Floating	X or Floating	L

2.5 Logic Diagram

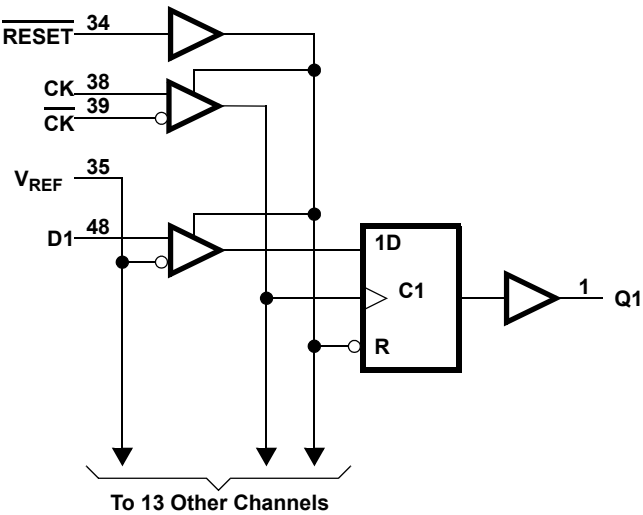


Figure 2 — Logic Diagram (Positive Logic)

## 2.6 Absolute Maximum Ratings

Supply voltage range, $V_{DD}$ or $V_{DDQ}$ .....	-0.5 V to 3.6 V
Input voltage range, $V_I$ (See Notes 2 and 3) .....	-0.5 V to $V_{DD} + 0.5$ V
Output voltage range, $V_O$ (See Notes 2 and 3) .....	-0.5 V to $V_{DDQ} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{DD}$ ) .....	$\pm 50$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{DDQ}$ ) .....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{DDQ}$ ) .....	$\pm 50$ mA
Continuous current through each $V_{DD}$ , $V_{DDQ}$ or GND .....	$\pm 100$ mA
Storage temperature range, $T_{STG}$ .....	-65 °C to 150 °C

NOTE 3 This value is limited to 3.6 V maximum.

			Min	Nom	Max	Unit
V <sub>DD</sub>	Supply voltage		V <sub>DDQ</sub>		2.7	V
V <sub>DDQ</sub>	Output supply voltage	PC1600-2700	2.3		2.7	V
		PC3200	2.5		2.7	V
V <sub>REF</sub>	Reference voltage (V <sub>REF</sub> = V <sub>DDQ</sub> / 2)	PC1600-2700	1.15	1.25	1.35	V
		PC3200	1.25	1.30	1.35	V
V <sub>TT</sub>	Termination voltage		V <sub>REF</sub> – 40 mV	V <sub>REF</sub>	V <sub>REF</sub> + 40 mV	V
V <sub>I</sub>	Input voltage		0		V <sub>DD</sub>	V
V <sub>IH</sub>	AC high-level input voltage	Data inputs	V <sub>REF</sub> + 310 mV			V
V <sub>IL</sub>	AC low-level input voltage	Data inputs			V <sub>REF</sub> – 310 mV	V
V <sub>IH</sub>	DC high-level input voltage	Data inputs	V <sub>REF</sub> + 150 mV			V
V <sub>IL</sub>	DC low-level input voltage	Data inputs			V <sub>REF</sub> – 150 mV	V
V <sub>IH</sub>	High-level input voltage	$\overline{\text{RESET}}$	1.7			V
V <sub>IL</sub>	Low-level input voltage	$\overline{\text{RESET}}$			0.7	V
V <sub>ICR</sub>	Common-mode input range	CK, $\overline{\text{CK}}$	0.97		1.53	V
V <sub>ID</sub>	Differential input voltage	CK, $\overline{\text{CK}}$	360			mV
I <sub>OH</sub>	High-level output current				–20	mA
I <sub>OL</sub>	Low-level output current				20	
T <sub>A</sub>	Operating free-air temperature		0		70	°C
NOTE 1	The $\overline{\text{RESET}}$ input of the device must be held at V <sub>DD</sub> or GND to ensure proper device operation. The differential inputs must not be floating, unless $\overline{\text{RESET}}$ is low.					



## 2 Device Standard (cont'd)

## 2.8 DC Specifications

**Table 5 — Electrical Characteristics over Recommended Operating Free-air Temperature Range for PC1600, PC2100, and PC2700**

PARAMETER		TEST CONDITIONS		V <sub>DD</sub>	MIN	TYP	MAX	UNIT
V <sub>IK</sub>		I <sub>I</sub> = -18 mA		2.3 V			-1.2	V
V <sub>OH</sub>		I <sub>OH</sub> = -100 μA		2.3 to 2.7 V	V <sub>DD</sub> - 0.2			V
		I <sub>OH</sub> = -16 mA		2.3 V	1.95			
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA		2.3 to 2.7 V			0.2	V
		I <sub>OL</sub> = 16 mA		2.3 V			0.35	
I <sub>I</sub>	All inputs	V <sub>I</sub> = V <sub>DD</sub> or GND		2.7 V			±5	μA
I <sub>DD</sub>	Static standby	$\overline{\text{RESET}}$ = GND		2.7 V			0.01	mA
	Static operating	$\overline{\text{RESET}}$ = V <sub>DD</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub>					†	
I <sub>DDD</sub>	Dynamic operating – clock only	$\overline{\text{RESET}}$ = V <sub>DD</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> , CK and $\overline{\text{CK}}$ switching 50% duty cycle		2.7 V			†	μA/ clock MHz
	Dynamic operating – per each data input	$\overline{\text{RESET}}$ = V <sub>DD</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> , CK and $\overline{\text{CK}}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.					†	μA/ clock MHz/ data input
r <sub>OH</sub>	Output high	I <sub>OH</sub> = -20 mA		2.3 to 2.7 V	7		20	Ω
r <sub>OL</sub>	Output low	I <sub>OL</sub> = 20 mA		2.3 to 2.7 V	7		20	Ω
r <sub>O(Δ)</sub>	r <sub>OH</sub> - r <sub>OL</sub>   each separate bit	I <sub>O</sub> = 20 mA, T <sub>A</sub> = 25 °C		2.5 V			4	Ω
C <sub>i</sub>	Data inputs	V <sub>I</sub> = V <sub>REF</sub> ± 310 mV		2.5 V	2.5		3.5	pF
	CK and $\overline{\text{CK}}$	V <sub>ICR</sub> = 1.25 V, V <sub>I(PP)</sub> = 360 mV			2.5		3.5	
	$\overline{\text{RESET}}$	V <sub>I</sub> = V <sub>DD</sub> or GND			†		†	
NOTE † The vendor must supply this value for full device description.								

**2 Device Standard (cont'd)****2.8 DC Specifications (cont'd)****Table 6 — Electrical Characteristics over Recommended Operating Free-air Temperature Range for PC3200**

PARAMETER		TEST CONDITIONS	V <sub>DD</sub>	MIN	TYP	MAX	UNIT
V <sub>IK</sub>		I <sub>I</sub> = -18 mA	2.5 V			-1.2	V
V <sub>OH</sub>		I <sub>OH</sub> = -100 µA	2.5 to 2.7 V	V <sub>DD</sub> - 0.2			V
		I <sub>OH</sub> = -16 mA	2.5 V	1.95			
V <sub>OL</sub>		I <sub>OL</sub> = 100 µA	2.5 to 2.7 V			0.2	V
		I <sub>OL</sub> = 16 mA	2.5 V			0.35	
I <sub>I</sub>	All inputs	V <sub>I</sub> = V <sub>DD</sub> or GND	2.7 V			±5	µA
I <sub>DD</sub>	Static standby	$\overline{\text{RESET}}$ = GND	2.7 V			0.01	mA
	Static operating	$\overline{\text{RESET}}$ = V <sub>DD</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub>				†	
I <sub>DDD</sub>	Dynamic operating - clock only	$\overline{\text{RESET}}$ = V <sub>DD</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> , CK and $\overline{\text{CK}}$ switching 50% duty cycle	2.7 V			†	µA/ clock MHz
	Dynamic operating – per each data input	$\overline{\text{RESET}}$ = V <sub>DD</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> , CK and $\overline{\text{CK}}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.				†	µA/ clock MHz data input
r <sub>OH</sub>	Output high	I <sub>OH</sub> = -20 mA	2.5 to 2.7 V	7		20	Ω
r <sub>OL</sub>	Output low	I <sub>OL</sub> = 20 mA	2.5 to 2.7 V	7		20	Ω
r <sub>O(Δ)</sub>	r <sub>OH</sub> - r <sub>OL</sub>   each separate bit	I <sub>O</sub> = 20 mA, T <sub>A</sub> = 25 °C	2.6 V			4	Ω
C <sub>i</sub>	Data inputs	V <sub>I</sub> = V <sub>REF</sub> ± 310 mV	2.6 V	2.5		3.5	pF
	CK and $\overline{\text{CK}}$	V <sub>ICR</sub> = 1.30 V, V <sub>I(PP)</sub> = 360 mV		2.5		3.5	
	$\overline{\text{RESET}}$	V <sub>I</sub> = V <sub>DD</sub> or GND		†		†	

NOTE † The vendor must supply this value for full device description.

## 2.9 Timing Requirements

			<b>PC1600, PC2100, PC2700</b>		<b>PC3200</b>		<b>UNIT</b>
			<b>V<sub>DD</sub> = 2.5 V ± 0.2 V</b>		<b>V<sub>DD</sub> = 2.6 V ± 0.1 V</b>		
			<b>MIN</b>	<b>MAX</b>	<b>MIN</b>	<b>MAX</b>	
f <sub>clock</sub>	Clock frequency			200		220	MHz
t <sub>w</sub>	Pulse duration, CK, $\overline{\text{CK}}$ high or low		2.5		2.5		ns
t <sub>act</sub> <sup>†</sup>	Differential inputs active time (see Note 1)			22		22	ns
t <sub>inact</sub> <sup>†</sup>	Differential inputs inactive time (see Note 2)			22		22	ns
t <sub>su</sub>	Setup time, fast slew rate (See Notes 3 and 5)	Data before CK ↑, $\overline{\text{CK}}$ ↓	0.65		0.65		ns
	Setup time, slow slew rate (See Notes 4 and 5)		0.9		0.75		
t <sub>h</sub>	Hold time, fast slew rate (See Notes 3 and 5)	Data after CK ↑, $\overline{\text{CK}}$ ↓	0.75		0.75		ns
	Hold time, slow slew rate (See Notes 4 and 5)		0.9		0.9		
NOTE † This parameter is not necessarily production tested.							
NOTE 1 Data inputs must be low a minimum time of t <sub>act</sub> max, after $\overline{\text{RESET}}$ is taken high							
NOTE 2 Data and clock inputs must be held at valid levels (not floating) a minimum time of t <sub>inact</sub> max, after $\overline{\text{RESET}}$ is taken low.							
NOTE 3 For data signal input slew rate ≥ 1 V/ns.							
NOTE 4 For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns.							
NOTE 5 CK, $\overline{\text{CK}}$ signals input slew rates are ≥ 1 V/ns.							

## 2 Device Standard (cont'd)

### 2.10 AC Specifications

**Table 8 — Switching Characteristics over Recommended Operating Free-air Temperature Range (unless otherwise noted) (see Figure 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	PC1600, PC2100, PC2700		UNIT
			V <sub>DD</sub> = 2.5 V ± 0.2 V		
			MIN	MAX	
f <sub>max</sub>			200		MHz
t <sub>pd</sub>	CK and $\overline{CK}$	Q	1.1	2.8	ns
t <sub>PHL</sub>	$\overline{RESET}$	Q		5	ns
t <sub>PDM</sub>	CK - $\overline{CK}$	QT	see Note 1		ns
NOTE 1 Measured with reference load, see Figure 4. t <sub>PDM</sub> is vendor specific. It is not required for compliant devices that this parameter is specified.					

**Table 9 — Switching Characteristics over Recommended Operating Free-air Temperature Range (unless otherwise noted) (see Figure 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	PC3200		UNIT
			V <sub>DD</sub> = 2.6 V ± 0.1 V		
			MIN	MAX	
f <sub>max</sub>			220		MHz
t <sub>pd</sub>	CK and $\overline{CK}$	Q	1.1	2.4	ns
t <sub>pdss</sub> (see Note 1)	CK and $\overline{CK}$	Q		2.7	ns
t <sub>PHL</sub>	$\overline{RESET}$	Q		5	ns
t <sub>PDM</sub>	CK - $\overline{CK}$	QT	see Note 2		ns
NOTE 1 The Simultaneous Switching specification is guaranteed by Characterization.					
NOTE 2 Measured with reference load, see Figure 4. t <sub>PDM</sub> is vendor specific. It is not required for compliant devices that this parameter is specified.					

### 3 Output Buffer Characteristics

#### 3.1 Voltage vs. Current (V/I)

The following table describes output-buffer Voltage vs. Current (V/I) characteristics that are sufficient to meet the requirements of registered DDR DIMM performance and timings. These characteristics are not necessarily production tested but can be guaranteed by design or characterization. Compliance with these curves is not mandatory if it can be adequately demonstrated that alternate characteristics meet the requirements of the registered DDR DIMM application.

**Table 10 — Output-buffer Voltage vs. Current (V/I) Characteristics**

Voltage (V)	Pull-down		Pull-up	
	I(mA)	I(mA)	I(mA)	I(mA)
	MIN	MAX	MIN	MAX
0	0	0	0	-0
0.1	5	18	-5	-18
0.2	10	30	-10	-30
0.3	15	44	-15	-44
0.4	19	55	-19	-55
0.5	23	67	-23	-67
0.6	27	78	-27	-78
0.7	30	90	-30	-90
0.8	34	101	-34	-98
0.9	36	112	-36	-106
1.0	38	121	-38	-113
1.1	40	131	-40	-119
1.2	42	140	-42	-125
1.3	43	150	-43	-130
1.4	44	159	-44	-134
1.5	44	167	-44	-137
1.6	45	176	-45	-140
1.7	45	184	-45	-143
1.8	45	192	-45	-146
1.9	45	199	-45	-149
2.0	45	206	-45	-152
2.1	46	212	-46	-154
2.2	46	218	-46	-156
2.3	46	222	-46	-157
2.4	46	226	-46	-159
2.5	46	229	-46	-160
2.6	46	233	-46	-161
2.7	46	234	-46	-162

### 3 Output Buffer Characteristics (cont'd)

#### 3.2 Slew Rate

The following table describes output-buffer slew-rate characteristics that are sufficient to meet the requirements of registered DDR DIMM performance and timings. These characteristics are not necessarily production tested but can be guaranteed by design or characterization. Compliance with these rates is not mandatory if it can be adequately demonstrated that alternate characteristics meet the requirements of the registered DDR DIMM application. This information does not necessarily have to appear in the device datasheet.

Obtain rise and fall time measurements by using the same procedure for obtaining “[Ramp]” data according to the current EIA IBIS specification. In particular it is very important to note that the following slew rates are specified at the output of the die, **without** package parasitics in the power, ground or output paths. The measurement points are at 20% and 80%. The slew-rate test load shall be a 50  $\Omega$  resistor to GND for Rise, and a 50  $\Omega$  resistor to  $V_{DDQ}$  for Fall. The  $dV/dt$  ratio is reduced to V/ns.:

**Table 11 — Output-buffer Slew Rate Characteristics**

<b>dV/dt</b>	<b>Min</b>	<b>Max</b>
<b>Rise</b>	1.1 V/ns	13.9 V/ns
<b>Fall</b>	1.1 V/ns	14.5 V/ns

#### 3.3 Simultaneous Switching

The vendor must supply, as requested, simultaneous switching information for full device description. In particular, slow corner propagation-delay increase due to simultaneous switching conditions is necessary for post-register timing analysis. This information does not necessarily have to appear in the device datasheet.

#### 4 Test Circuit and Switching Waveforms

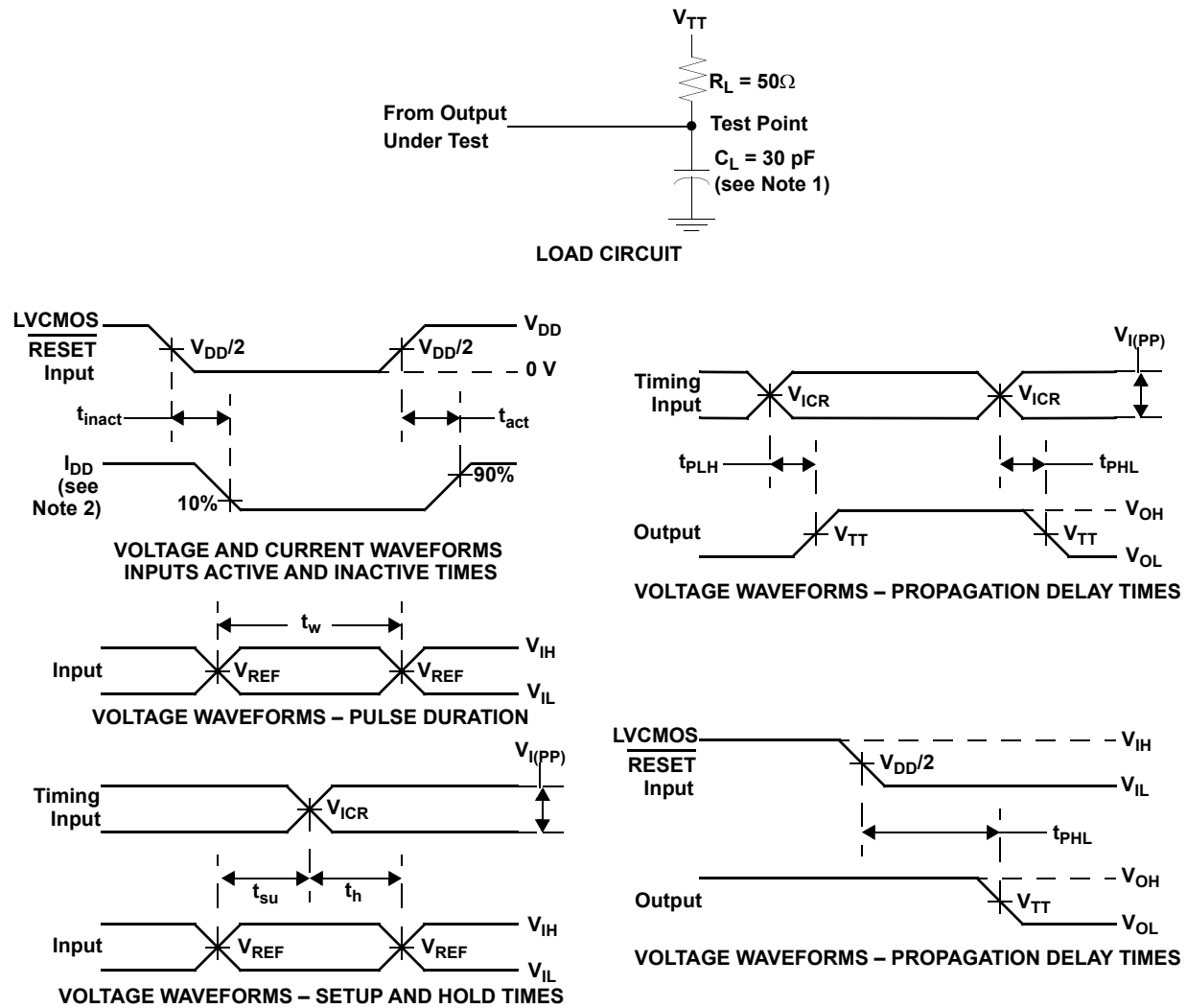


Figure 3 — Parameter Measurement Information

NOTE 1  $C_L$  includes probe and jig capacitance.

NOTE 2  $I_{DD}$  tested with clock and data inputs held at  $V_{DD}$  or GND, and  $I_O = 0$  mA.

NOTE 3 All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ , input slew rate =  $1$  V/ns  $\pm 20\%$  (unless otherwise specified).

NOTE 4 The outputs are measured one at a time with one transition per measurement.

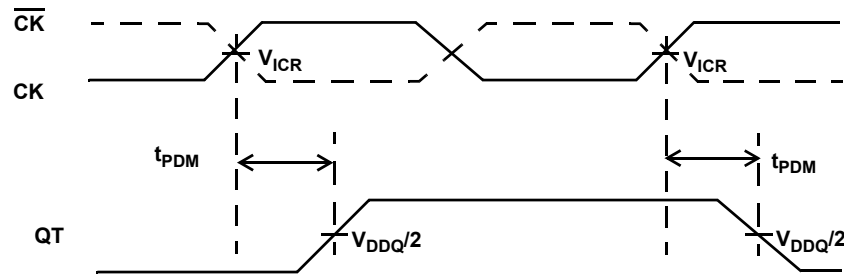
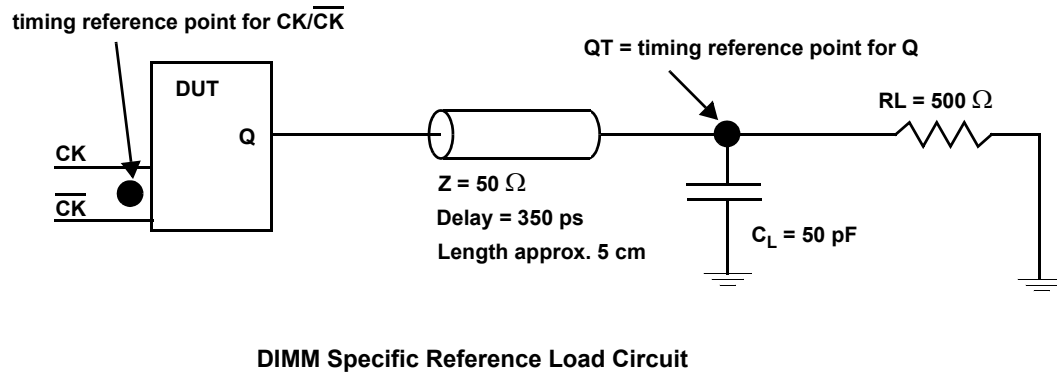
NOTE 5  $V_{TT} = V_{REF} = V_{DDQ}/2$

NOTE 6  $V_{IH} = V_{REF} + 310$  mV (ac voltage levels) for differential inputs.  $V_{IH} = V_{DD}$  for LVC MOS input.

NOTE 7  $V_{IL} = V_{REF} - 310$  mV (ac voltage levels) for differential inputs.  $V_{IL} = \text{GND}$  for LVC MOS input.

NOTE 8  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

## 5 Reference Load for Registered DIMMs



**Figure 4 — Measurement Setup for  $t_{PDM}$**

NOTE 1 The transmission line should be designed to have an impedance equal to  $50\ \Omega$  and a delay (in matched impedance environment) equal to 350 ps. The actual length may vary with PCB parameters.

## 6 Reference to other Applicable JEDEC Standards and Publications

- JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products*.
- JEP104-A, *Reference Guide to Letter Symbols for Semiconductor Devices*.
- JESD8-5, *2.5 Volt  $\pm 0.2$  V (Normal Range) and 1.8 V to 2.7 V (Wide Range) Power Supply Voltage and Interface for Non-terminated Digital Integrated Circuits*.
- JESD8-9, *Stub Series Terminated Logic for 2.5 V (SSTL\_2)*.
- JESD21-C, *Configuration for Solid State Memories*.



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**Annex A — (Informative) Differences between JESD82-3B and JESD82-3A**

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The following list briefly describes most of the changes made to entries that appear in this publication, JESD82-3B, compared to its predecessor, JESD82-3B (October 2002). If the change to a concept involves any words added or deleted, it is included. Punctuation changes may not be included.

**Page    Description of change**

- |   |   |
|---|---|
| 4 | Table 4: Added PC3200 values for Vddq and Vref                |
| 6 | Table 6 has been added, Electrical characteristics for PC3200 |
| 7 | Table 7 - Added specifications for PC3200                     |
| 9 | Table 9 has been added, Switching characteristics             |

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**Annex B — (Informative) Differences between JESD82-3B.01 and JESD82-3B**

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Editorial changes as follows:

1. Terminology update: Table 1 - Changed “master” to “main” for description of CK and  $\overline{\text{CK}}$
2. Updated JEDEC logos and Standard Improvement Form
3. All section headings, table titles, and figure titles changed to Initial Caps
4. Table layouts updated to JEDEC standard format

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## Standard Improvement Form

**JEDEC No. JESD82-3B.01**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC  
Attn: Publications Department  
3103 North 10th Street, Suite 240 South  
Arlington, VA 22201-2107

Fax: 703.907.7583

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1. I recommend changes to the following:

☐ Requirement, clause number \_\_\_\_\_

☐ Test method number \_\_\_\_\_ Clause number \_\_\_\_\_

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other \_\_\_\_\_

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2. Recommendations for correction:

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3. Other suggestions for document improvement:

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Submitted by

Name: \_\_\_\_\_

Phone: \_\_\_\_\_

Company: \_\_\_\_\_

E-mail: \_\_\_\_\_

Address: \_\_\_\_\_

City/State/Zip: \_\_\_\_\_

Date: \_\_\_\_\_

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